

**NEW UTILITY PATENT APPLICATION  
TRANSMITTAL**Docket No.  
M4065.0127/P127-ATotal pages in this  
submission

(Only for new nonprovisional applications under 37 C.F.R. 1.53(b))

**TO THE ASSISTANT COMMISSIONER FOR PATENTS****Box Patent Application  
Washington, D.C. 20231**

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

**SILICON MULTI-CHIP MODULE PACKAGING WITH INTEGRATED PASSIVE COMPONENTS  
AND METHOD OF MAKING**

and invented by:

Kie Y. Ahn and Leonard Forbes

**IF A CONTINUATION APPLICATION**, check appropriate box and supply requisite information:☐ Continuation ☒ Divisional☐ Continuation-in-part (CIP) of prior application No.: 09/241,061

Enclosed are:

**Application Elements**

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 42 pages(s) and including the following:
  - a. ☒ Descriptive title of the invention
  - b. ☐ Cross references to related applications (*if applicable*)
  - c. ☐ Statement regarding Federally-sponsored research/development (*if applicable*)
  - d. ☐ Reference to microfiche appendix (*if applicable*)
  - e. ☒ Background of the invention
  - f. ☒ Brief summary of the invention
  - g. ☒ Brief description of the drawings (*if drawings filed*)
  - h. ☒ Detailed description
  - i. ☒ Claims as classified below
  - j. ☒ Abstract of the disclosure

**Application Elements (continued)**

3. ☒ Drawing(s) (when necessary as prescribed by 35 U.S.C. 113)  
☒ Formal ☐ Informal Number of sheets: 7
4. ☒ Oath or Declaration  
a. ☐ Newly executed (original or copy) ☐ Unexecuted  
b. ☒ Copy from a prior application (37 C.F.R. 1.63(d) (for continuation/divisional applications only)  
c. ☐ With Power of Attorney ☒ Without Power of Attorney
5. ☒ Incorporation by reference (usable if Box 4b is checked)  
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer program in microfiche
7. ☐ Genetic sequence submission (if applicable, all must be included)  
a. ☐ Paper copy  
b. ☐ Computer readable copy  
c. ☐ Statement verifying identical paper and computer readable copies

**Accompanying Application**

8. ☐ Assignment papers (cover sheet & document(s))
9. ☒ 37 C.F.R. 3.73(b) statement (when there is an assignee)
10. ☐ English translation document (if applicable)
11. ☒ Information Disclosure Statement/PTO-1449 ☒ Copies of IDS citations
12. ☒ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☐ Certified copy of priority document(s) (if foreign priority is claimed)
15. ☐ Certificate of Mailing  
☐ First Class ☐ Express Mail (Label No.: \_\_\_\_\_)
16. ☐ Small Entity statement(s) -- # submitted \_\_\_\_\_ (if Small Entity status claimed)

**Accompanying Application (continued)**

- 17.
- ☐
- Additional enclosures (please identify below):

**Fee Calculation and Transmittal**

The filing fee for this utility patent application is calculated and transmitted as follows:

- ☒
- Large Entity
- ☐
- Small Entity

<b><u>CLAIMS AS FILED</u></b>						
<b>For</b>	<b># Filed</b>	<b># Allowed</b>	<b># Extra</b>	<b>Rate</b>		<b>Fee</b>
<b>Total Claims</b>	35	- 20 =	15	x	\$18.00	\$270.00
<b>Independent Claims</b>	1	- 3 =		x	\$78.00	
<b>Multiple Dependent Claims (check if applicable)</b> <input type="checkbox"/>						
<b>Other Fees (specify purpose):</b>						
<b>BASIC FEE</b>						\$690.00
<b>TOTAL FILING FEE</b>						\$960.00

- ☒ A check in the amount of \$960.00 to cover the total filing fee is enclosed.
- ☒ The Commissioner is hereby authorized to charge and Deposit Account No. 4 - 1073 as described below. A duplicate copy of this sheet is enclosed.
- ☐ Charge the amount of \_\_\_\_\_ as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.31(b).


Dated: September 12, 2000

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PATENT

Docket No.: M4065.0127/P127-A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:  
Kie Y. Ahn et al.

Serial No.: (Not Yet Assigned - Divisional  
of Serial No. 09/241,061)

Group Art Unit: 2815

Filed: Concurrently Herewith

Examiner: S. Clark

For: SILICON MULTI-CHIP MODULE  
PACKAGING WITH  
INTEGRATED PASSIVE  
COMPONENTS AND METHOD  
OF MAKING

Assistant Commissioner for Patents  
Washington, D.C. 20231

FIRST PRELIMINARY AMENDMENT

Dear Sir:

Prior to examination on the merits, please amend the above-identified U.S. patent application as follows:

**In the Specification:**

Page 1, line 3, before "Field of the Invention" please add -- This application is a divisional application of application Ser. No. 09/241,061 filed on February 1, 1999, now U.S. Patent No. \_\_\_\_, which is hereby incorporated by reference. --

**In the Claims:**

Please cancel claims 1-87.

**REMARKS**

The Specification has been amended to provide reference to the parent application. Claims 1-87 have been cancelled. Claims 88-123 are pending in this application.

Favorable consideration of the application is respectfully requested.

Dated: September 12, 2000

Respectfully submitted,

By 

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Docket No.: M4065.127/P127  
Micron Ref.: 98-0747/US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
APPLICATION FOR U.S. LETTERS PATENT

Title:

**SILICON MULTI-CHIP MODULE PACKAGING WITH INTEGRATED  
PASSIVE COMPONENTS AND METHOD OF MAKING**

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**SILICON MULTI-CHIP MODULE PACKAGING WITH INTEGRATED  
PASSIVE COMPONENTS AND METHOD OF MAKING****BACKGROUND OF THE INVENTION**5      **1. FIELD OF THE INVENTION**

This invention relates to multiple function semiconductor devices and, in particular, to silicon packaging for holding semiconductor devices and passive electronic components in close proximity.

10      **2. DESCRIPTION OF THE RELATED ART**

Portable wireless communications are a rapidly growing segment of consumer communication devices which are designed to operate in the radio frequency (RF) range. Many of these devices now operate in the L-band, or  
15      between 1-2.4 Gigahertz. In light of the increased demand for RF devices and the numerous digital-based communications systems which are currently available, an integrated package capable of delivering RF and digital communications has become desirable. Integrated portable communications devices would allow users to utilize one device for operating in a variety of  
20      communications systems. In addition, the integration of components offers attractive savings in terms of packaging size, cost, and energy requirements when compared to the operation of electrically and physically separate systems within one device.

The successful integration of RF devices into known digital communications systems requires the implementation of RF components within digital systems. The group of essential RF components, the front end circuitry of RF devices, generally includes passive electronic components. One of the  
5 benefits of using passive components in front end circuitry is that they experience relatively low loss due to the absence of noise from power sources. In addition, passive components may be processed at low cost using relatively few steps and common materials. Passive components include inductors, capacitors, and resistors. These components may be used to provide RF tuned amplifiers,  
10 oscillators, and optimizing broad-band filters which are required in RF communication systems.

Integrating RF and digital circuitry on a single package will place restrictions upon the composition and construction of the included components. A key component to the viability of personal communication and similar devices  
15 is the conservation of power to preserve battery life. Therefore, integrated digital and RF components, such as inductors, resistors and capacitors, should be able to operate in low power environments. The restriction of having a low power supply has, in the past, limited the advance of integrated systems.

In addition, the production of an integrated package would  
20 theoretically be optimized by using known integrated circuit (IC) processes for the manufacture of such systems. The existence of a variety of known IC



fabrication processes in addition to the inherent speed, low power consumption, and reduced size of IC make it ideal for use in integrated devices.

Resistors and capacitors form the building blocks of a variety of RF devices. The resistivity of a material is dependant upon its composition and environment. For RF applications, resistors must have precise, low fluctuation resistivity values. For use in RF devices a resistor must be able to operate at relatively low resistivity values due to the reduced voltage available from a power supply as compared to non-integrated IC devices. Similarly, capacitors for RF devices must have predictable values with low tolerances. Construction of capacitors and resistors for use in an integrated system while retaining the necessary RF characteristics is problematic due to the opposing concerns of RF-constrained component operating parameters with the size and power supply parameters of integrated circuits.

The most challenging RF component to adapt to an integrated system is the inductor. Inductors are an essential component of a variety of RF devices, including RF amplifiers which employ a tuned load. RF amplifiers supply gain using inductor-capacitor resonance to nullify device and parasitic capacitance at the center frequency. Such devices also form a secondary filter for noise and out-of-band signals. Inductors in integrated systems must be able to provide relatively large inductance values, ideally greater than 10 nH (dependent upon frequency range) while being physically small such that a compact architecture can be achieved. The inductance value is dependent in large part upon the

geometry of the inductor itself. In fact, the inclusion of passive components will often dictate the size of system more than any other part. Thus, design of high valued inductors within compact spaces is necessary for successful RF/digital integration.

5                   Capacitors and inductors in RF front end circuitry must also be tuned to deliver high quality (Q) factors at the operational frequency. A Q factor is dependent upon resistance and either capacitance or inductance, depending upon the component being measured. Maximizing Q while recognizing the necessary limitations set by theoretically effective integrated systems (size, power, etc.) has  
10                   proven difficult. In addition, inductors and capacitors experience rapid deterioration of performance near their self resonating frequency. A self resonating frequency will vary depending upon the material composition, the size of the device, and the devices surroundings. Many current RF systems operate at frequencies ranging from 1.0 to 2.5 GHz. Therefore, the self resonating  
15                   frequency of a inductor or capacitor element should be significantly higher than the operating frequency to avoid deterioration of the effectiveness of the element.

                  Various methods have been used to integrate RF components into IC processes. Gallium-Arsenide (GaAs) substrates are the most common platforms  
20                   for fabricating RF passive devices in currently known systems. GaAs has several beneficial qualities which make it attractive for use in integrating RF components. Due to the semi-insulating qualities of GaAs, certain passive

elements having low to medium Q factors (5-15) may be placed on chip without experiencing severe effect deterioration. However, GaAs-based RF components suffer from limited Q factors due to inherent problems with on-chip noise and physical limitations. In addition, the on-chip noise contributes to increased  
5 fluctuations in inductance and capacitance values, rendering them fairly unpredictable. The resulting GaAs-based systems exhibit properties which are unacceptable if the device is to function in future integrated communications networks which will require predictability and high Q factors.

Silicon-based passive components theoretically offer the best  
10 combination of qualities for use in integrated systems. Silicon is a relatively inexpensive material for which numerous processing systems have been developed. Silicon bipolar processes have threshold frequencies, from 2-50 GHz, which are sufficient to supply gain through the most common RF communications frequencies. In addition, silicon IC's are capable of higher  
15 complexity than GaAs systems, allowing for the possibility of more compact integration.

Though attractive, silicon technology raises several barriers to successful integration of RF and digital technology. Silicon substrates suffer from lower substrate resistivity when compared to GaAs. The inherent  
20 conductance of the silicon substrate induces loss and limits inductors and capacitors to poor Q factors. Encasing the transmission line conductors in the oxide insulators used in silicon integrated circuits increases the stray capacitance

and lowers the self resonance frequency. Thus, as the frequency received by an integrated communications system is increased, the inductance will decrease. Losses in the conductive silicon substrates are increased by the high dielectric constant of the insulators under the conductors, and relatively large values of stray capacitive coupling to the silicon substrate. Resistors, though effected by their surroundings, generally perform well when deposited on a silicon substrate. Poor Q value in capacitors and inductors and RF/digital line conductor loss have created significant barriers to fabrication of a viable integrated system. Though several attempts to solve these problems have been made, no device has addressed each of these concerns sufficiently. The effect of a silicon substrate on passive device performance is described in Integrated Passive Components in MCM-Si Technology and their Applications in RF-Systems, IEEE 1998 International Conference on Multichip Module and High Density Packaging, 1998 (*Hartung*). A multilayer construction containing a one micron thick silicon dioxide layer as an insulator was formed on a silicon substrate and significant performance loss was found in passive devices formed within the multilayer construction due to the low resistivity of the silicon substrate.

Several prior art schemes have been developed to deal with problems inherent in silicon-based passive element fabrication and integration. One solution utilizes an air bridge between an inductor and the silicon substrate as described in U.S. Patent 5,539,241 (*Abidi et al.*). Fig. 8 shows a typical air bridge construction wherein a cavity 254 is etched in substrate 250. Inductor elements 256 are then deposited in oxide layer 252 such that the inductor

elements 256 are located above the cavity 254. The cavity 254, filled with air, acts as an insulator between the inductors 256 and the semiconductor substrate 250 and, therefore, reduces the negative effects which come from having a silicon substrate.

5 Similarly, the use of suspended wire spans is described in A 1V, 5mW, 1.8GHz, Balanced Voltage-Controlled Oscillator with an Integrated Resonator (*Hitko, et al.*), to create inductors for use in silicon-based voltage controlled oscillators (VCO). Shown in Fig. 9a and 9b, the design is comprised of metal wires 304 suspended from the surface of the substrate 300 by the use of pads  
10 302. The wires 304 are formed in a U shape, shown in Fig. 9b, and are suspended above substrate 300 such that air acts as an insulator between the silicon substrate 300 and the wires 304. The metal wires 304 are electrically connected to circuit elements contained within the substrate 300 through contacts 306.

15 Higher Q inductors have also been developed in silicon-based substrates using a five to six level metal BiCMOS technology, as described in Integrated RF and Microwave Components in BiCMOS Technology, 43 IEEE Transactions on Electron Devices 9, 1996 (*Burghartz*). However, the  
20 implementation of spiral inductors using this technology is not practical in light of the fact that the five to six levels of metal architecture needed is far in excess of the two to four levels most commonly used in CMOS construction processes.

Integration of spiral inductors has also been accomplished for discrete multi-chip modules (MCM-D) using LSI technology. As described in Low-Complexity MCM-D Technology with Integrated Passives for High Frequency Applications, IEEE 1998 (*Samber et al.*), the process uses a double metal back-  
5 end process on isolated high-ohmic silicon and incorporates a resistor layer, thin film resistors, capacitors, and inductors.

Integration of passive components into MCM-Si technology has proven to be difficult. Silicon is preferred because it is relatively easy to process, there are known methods for processing, and it achieves good flatness and  
10 reduced roughness over comparable materials. Passive devices in silicon would also have similar thermal coefficients to the chip die, ensuring environmental compatibility. U.S. Patent 5,770,476 teaches the use of an interposer constructed of a conductor-insulator-conductor on which passive devices are created. None of the described methods produces silicon-based system within  
15 which high-Q inductors and capacitors can be placed in close proximity to a chip containing digital circuitry.

### SUMMARY OF THE INVENTION

The present invention provides a multi-chip module that is able to  
20 overcome some of the problems attendant the integration of RF and digital circuitry within the same packaging.

The above and other features and advantages of the invention are achieved by providing an apparatus for the supply of passive electronic elements to a chip containing circuitry capable of operating in a digital-based communications system. The invention provides a silicon interposer chip

5 package which includes a silicon substrate and which is capable of carrying one or more IC chips and which does not suffer semiconductor leeching problems. A silicon substrate is formed from a silicon layer and an insulating layer, the latter of which is preferably constructed of oxide. Passive circuit elements are fabricated within and/or on the interposer insulating layer. Integrating the

10 passive circuit elements within and/or on the interposer insulating layer and the connection of the interposer with an integrated circuit chip increases the overall efficiency of the device. The interposer is bonded to the integrated circuit chip using flip-chip processing. The resulting silicon based CMOS package has passive circuit elements having superior Q factors and exhibits an overall increase

15 in mechanical strength in comparison to most known methods for integrating RF integrated circuit components.

The above and other advantages and features of the present invention will be better understood from the following detailed description of the preferred embodiment which is provided in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross sectional view of a preferred embodiment of the present invention;

5 Fig. 2a-c are cross sectional views depicting the fabrication of an interposer shown in Fig. 1;

Fig. 3 is a cross-sectional view of an integrated circuit chip shown in Fig. 1;

10 Fig. 4 is a cross sectional view of the Fig. 1 arrangement just prior to bonding of various elements together;

Fig. 5 is a perspective view of a substrate containing a plurality of interposers which are to be diced therefrom;

Fig. 6 is a cross sectional view of Fig. 1 structure encapsulated with a lead frame;

15 Fig. 7 is a perspective view of an RF/digital communications system utilizing the Fig. 6 structure;

Fig. 8 is a cross sectional view of a prior art inductor element utilizing an air bridge; and



Figs 9a-b are side and top views of a prior art inductor element utilizing wire spans.

#### DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced.

These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized, and that structural, logical and electrical changes may be made without departing from the spirit and scope of the present invention. Wherever possible, like numerals are used to refer to like elements and functions in the various figures of the drawings and between the different embodiments of the present invention.

An integrated circuit chip package 30 in accordance with the present invention is illustrated generally in Fig. 1. Package 30 consists of an interposer 10 and integrated circuit ("IC") chips 20, 22. To allow for the integration of active and passive circuit elements in a package 30 having a compact architecture, the interposer 10 has a substrate layer 100 and an insulating layer 104 which may be formed on one or both sides of substrate layer 100. Passive circuit elements, represented in the embodiment of Fig. 1 as inductors 106, resistors 108, and capacitors 110 are formed in and/or on the insulating layers 104. The passive circuit elements are separated from the substrate layer 100 by a barrier layer 170

of the insulating layer 104. Though shown in Fig. 1 as inductors 106, resistors 108, and capacitors 110, the passive circuit elements contained within interposer 10 may be any device which does not require an external power source for operation. Passive elements on the same side of the interposer 10 are interconnected by conductor lines 112, which are preferably metal lines. The integrated circuit chips 20, 22 are comprised of chips 120 which contain at least one integrated circuit element 140 and conductor lines 142, which are also preferably metal lines, to form an electrical connection between the integrated circuit elements 140 and from the integrated circuit elements 140 to solder joints 150. The IC chips 20 are preferably flip-chip mounted onto interposer 10 though solder joints 150 which connect conductor lines 112 of the interposer 10 to conductor lines 142 of the chips 120. A wire bond 138 or a lead frame may be connected to either the IC chips 20, 22 or the interposer 10 to facilitate connection of the package 30 to an outside source, such as a circuit board 184 or another package 30. As shown in Fig. 1, the open spaces between the IC chips 20, 22 and the interposer 10 is filled with an epoxy 122. The epoxy 122 provides for passivation and improves the fatigue characteristics of the solder joints 150 which exist between the IC chips 20, 22 and the interposer 10.

Silicon is a particularly suitable material for forming the substrate 100 of interposer 10. Silicon is inexpensive and readily available. Further, the material characteristics of silicon, specifically the thermal characteristics, match those of IC chips 20, 22 which are commonly formed of silicon. In addition to

silicon, gallium arsenide (GaAs) may also be used for the substrate 100 of the interposer 10.

The insulating layer 104 exists on one or both sides of the substrate 100 and forms an effective barrier layer 170 between the passive elements, e.g. the inductors 106, the capacitors 110 and the resistors 108, and the substrate 100. The formation of the barrier layer 170 prevents effect degradation of the inductors 106, the capacitors 110 and the resistors 108 by eliminating loss caused by the inherent conductance of the semiconductor substrate 100. In the embodiment in which substrate layer 100 is formed of silicon, the insulating layer 104 may be a silicon-oxide ( $\text{SiO}_2$ ) layer which is formed on one or both sides of a silicon substrate 100 such that the inductors 106, the capacitors 110 and the resistors 108 are shielded from the silicon substrate 100 by a barrier layer 170 of the insulating layer 104 sufficient to eliminate conductance to the substrate 100.

IC chips 20, 22 may be any CMOS-based chips containing logic device elements such as transistors. For example, the IC chips 20, 22 may be a storage device such as a memory chip, a microprocessor chip. Alternatively, the IC chips 20, 22 may contain analog circuits or a combination of analog and digital circuits. In one preferred embodiment IC chips 20, 22 are provided which contain digital-based communication circuitry. Each of the IC chips 20, 22 contains a plurality of integrated circuit elements 140 and interconnecting conductor lines 142 which also connect with solder joints 150. Chip 120 may be constructed using a silicon substrate, a GaAs substrate, or any other material

substrate known for use in integrated circuit fabrication. The digital circuit elements 140 may be transistor elements such as MOSFET transistors. In one embodiment of the present invention, the digital circuit elements 140 of the chips 120 form the required analog and digital circuitry for an analog/digital RF communication system.

The process for forming package 30 will next be described with reference to Figs. 2a-5. Fig. 2a shows the interposer 10 in a preliminary stage of construction having a substrate 100 and insulating layers 104 on opposite sides of the substrate 100. The substrate 100, which may ultimately yield many interposers 10, is subjected to an oxide deposition, preferably silicon dioxide ( $\text{SiO}_2$ ) on a silicon substrate 100. Oxide deposition may occur through methods known in the art, for example thermal oxidation, chemical vapor deposition, and sputtering techniques. The oxide deposition process forms an insulating layer 104 on both major surfaces of the silicon substrate 100. The insulating layer 104 is thin in comparison to the substrate 100, for example, the insulating layer 104 may be between 3-5 microns thick for a substrate 100 having a thickness of 50 microns.

Alternatively, insulating layer 104 may be formed on only one or a part of one or both surfaces of the substrate layer 100, as desired. For purposes of further description of the invention an interposer 10 having insulating layers 104 on both sides of substrate 100 will be discussed.

Referring now to Figs. 2b and 2c, once the insulating layers 104 have been formed, inductors 106, resistors 108, and capacitors 110 and metal interconnect lines 112 are formed in and on an upper surface of the insulating layers 104 through a variety of techniques, described below. A barrier layer 170 of insulating layer 104 remains between the inductors 106, resistors 108, capacitors 110, and conductor lines 112 and the substrate 100 sufficient to shield the inductors 106, resistors 108, capacitors 110, and conductor lines 112 from the conductance of the substrate 100. The formation of the inductors 106, resistors 108, capacitors 110, and conductor lines 112 may be accomplished in any order and will be dictated by the desired number and placement of passive elements within the interposer 10.

The resistors 108 are preferably thin-film, precision valued resistors. Utilizing thin film construction for the resistors 108 simplifies the construction of the package 30 while allowing a compact architecture to be maintained. The resistors 108 may be formed on the surface of insulating layer 104 by film deposit, masking sequences, or by lift-off techniques. The resistors 108 may be formed of any metallic material having the desired resistance characteristics such as, for example, nichrome, titanium, or tungsten. The reduction in size and weight possible with thin film techniques is complemented by the fact that wire bonds are not needed since there is direct metallization contact through conductor lines 112 to the resistors 108, as shown in Fig. 2c. This results in

compact architectures and improved performance due to a reduction in the parasitic effects attributed to wire bonds.

The capacitors 110 are also constructed using thin film processes such as, for example, film deposit, masking sequences or lift-off techniques. The capacitors 110 are preferably metal-dielectric-metal capacitors each formed by depositing a pair of metal layers, the storage node 126 and the cell plate 128, separated by a deposited dielectric layer 130. The storage node 126 and the cell plate 128 are preferably formed of a metallic material and may vary in size dependant upon the desired storage capacity of the individual capacitors 110. Storage node 126 is required as the substrate 100 cannot act as part of the capacitor 110 due to the thickness of barrier layer 170. The storage node 126 is electrically connected to other passive elements and solder joints 150 through conducting lines 112, preferably metal lines, deposited prior to deposition of the storage node 126. The dielectric layer 130 is preferably another layer of oxide similar to that which forms insulating layer 104 and is grown after deposition of the storage node 126. The dielectric layer 130 may be, for example, a thin silicon dioxide layer having a thickness of less than 1500 Å. Alternatively, the dielectric layer 130 may be comprised of an oxide-nitride-oxide dielectric which would allow the capacitors 110 to occupy a smaller overall area. The insulating layer 104 is then grown through oxide deposition to encase the capacitors 110. To allow electrical contact to the capacitors 110, wells 134 are etched into insulating layer 104 such that the cell plates 128 are exposed. The wells contain

conductors connected to conducting lines 112. Because the capacitors 110 are completely encased in the insulating layer 104, the present invention is mechanically stronger than other passive element constructions, such as those using the air-bridge construction shown in Fig. 8.

5           The inductors 106 are preferably metal spiral inductors formed by deposition of a thin metallic layer in a spiral shape after formation of the barrier layer 170 of the insulating layer 104, as shown in Fig. 2b. This is followed by additional oxide growth of insulating layer 104 such that the inductors 106 are encased by insulating layer 104. Spiral inductors are thin strips of metal formed  
10           in a spiral shape parallel to the plane of the surface of insulating layer 104. The benefit of using spiral inductors for the passive element inductors 106 is that a significant reduction in overall size is possible, in comparison to non-spiral inductors, which reduces resistance in the inductors 106 and, therefore, results in higher Q factors for the inductors 106. The inductors 106 may be formed by  
15           any number of known techniques such as sputtering, evaporation, chemical vapor deposition, physical vapor deposition, etc. As noted, after deposition of the inductors 106, the insulating layer 104 is grown to encase the spiral inductor 106 as shown in Fig. 2b and 2c. To allow electrical contact to the inductors 106, wells 132 are etched into the insulating layers 104 such that a portion of  
20           the inductors 106 is exposed for electrical connection to conducting lines 112.

Referring to Fig. 2c, the inductors 106, resistors 108, and capacitors 110 of the interposer 10 are electrically connected by conductor lines 112, preferably

metal lines, which may be formed at varying points in the processing of interposer 10, as needed. Conductor lines 112 form a 'bus' for connecting the inductors 106, resistors 108, capacitors 110, and any other elements situated on or within the insulating layers 104 of the interposer 10. To form an electrical contact to the inductors 106 and capacitors 110 the conductor lines 112 must fill wells 132, 134, respectively. Conductor lines 112 may be constructed of, for example, aluminum (Al), copper (Cu), or silver (Ag) deposited by masked sputtering, evaporation, chemical vapor deposition, or physical vapor deposition techniques. Although the conductor lines 112 are shown in Figs. 1, 2c, and 3 to consist of one layer of metal, any number of conductor lines 112 may be deposited on any number of insulating layers as are needed for circuit connection depending upon the placement of passive or active devices within the interposer 10.

In another embodiment of the invention, a polyamide film is used to construct insulating layer 104 instead of an oxide material. The inductors 106, resistors 108, capacitors 110, and conductor lines 112 are deposited in the polyamide film layer 104 through flex circuit manufacturing processes. Polyamide may be preferred to oxide in cases where lower capacitance is required. In addition, polyamide offers insulating capabilities similar to oxides but with a lower required thickness which reduces the overall size of package 30. Therefore, the use of polyamide film layers 104 may further shrink the geometry of integrated communications systems utilizing the present invention.



When the present invention is used in digital/analog RF communications systems, the inductors 106, resistors 108 and capacitors 110 are formed such that the passive RF circuitry is formed in the interposer 10. The passive elements may also be formed on the surface of the insulating layer 104. The capacitor 110, resistor 108 and inductor 106 may also be used as components in the implementation of RF circuits including, for example, oscillators, tuned amplifiers, and broad band amplifiers.

Although Figs. 1-2, and 4 generally show one inductor 106, resistor 108, and capacitor 110 on or within the insulating layers 104 on each surface of the substrate 100, any number or combination of passive circuit elements may be used on one or both sides of the substrate 100. Alternatively, the interposer substrate 100 may also have active devices built on or into the insulating layers 104 on one or both sides of the substrate 100. At a minimum, interposer 10 has at least one passive element on one surface thereof and a barrier layer 170 between the passive elements and substrate 100.

To facilitate connection of the interposer 10 to the IC chips 20, 22, solder ball leads 118 are formed on interposer 10 as shown in Fig. 2c. The connection of the solder ball leads 118 to the interposer 10 is accomplished by placing solder balls on pads connected to conductor lines 112 of the interposer 10 such that an electrical connection is made between the conductor lines 112 and the solder ball leads 118 at selected points. Similarly, solder balls 126 are formed on the surface of a chip 120 such that electrical connection to integrated

circuit elements 140 is established through conducting layer 142 as shown in Figs. 3 and 4. The solder ball leads 118, 126 are, preferably, composed of Cr-Cu-Au, Zr-Ni-Cu-Au, Ti-Ni-Cu-Au, or lead-based (Pb) composites. If a global heating method is to be used, wherein the temperature of the entire package 30 is raised to a temperature sufficient to melt the solder ball leads 118, 126, the use of different types of solder having different melting points may be desirable to form individual or groups of solder ball leads 118 and 126. For example, Pb 2.5% solder may be used for the solder ball leads 118, 126 on one surface of the interposer 10, and Pb 11% solder may be used for the solder ball leads 118, 126 for the other surface of interposer 10. Further, another different type of solder, for example Pb-62% Sn, may be used for soldering the interposer 10 into a circuit board. Alternatively, the solder ball leads 118, 126 are heated locally so that the heating of one solder joint 150 does not cause heating of other solder joints 150, such as those on the opposing surface of the interposer 10.

After the interposer 10 has been constructed and the IC chips 20, 22 have been provided, the interposer 10 is ready to have the IC chips 20, 22 mounted on its opposing surfaces. The packaging system 30 of the present invention is formed by mounting the IC chips 20, 22 to the interposer 10 by a process often called "flip chip" bonding, as shown in Figs. 1 and 4. The interposer 10 and IC chips 20, 22 are arranged ( or "flipped") with solder ball leads 118 touching corresponding solder ball leads 126 on interposer 10 and IC chips 20, 22, respectively, as shown in Fig. 4. The solder ball leads 118 and 126 are then

heated to or above the melting point temperature of the specific solder material used such that solder joints<sub>150</sub> are formed, as shown in Fig. 1.

Using a “flip chip” manufacturing method allows for the production of high-density device assemblies. The assembly method places the passive device  
5 elements, inductors 106, resistors 108, and capacitors 110, in close physical proximity to the circuitry contained within IC chips 20, 22 to reduce the overall size of package 30. Therefore, the compact architecture needed to successfully integrate RF and digital circuitry can be realized. Although Fig. 4 shows interposer 10 and each IC chip 20, 22 having two solder ball leads 118, 126,  
10 respectively, any number of solder ball leads may be formed on the interposer 10 and IC chips 20, 22 depending upon the number of electrical connections required between the interposer 10 and the specific IC chips 20, 22 used in the package 30.

As an alternative to the use of solder balls 118, 126, a conductive adhesive  
15 may be used to attach the IC chips 20, 22 to the interposer 10, thereby avoiding any problems associated with heating.

In yet another embodiment of the invention, a single semiconductor substrate may be used to form interposers 10. Fig. 5 shows a product 50 having a silicon substrate layer 200 and insulating layers 206 which have been processed  
20 to form a number of interposers 10 according to the present invention. The product 50 may then be diced along lines 202, 204 to form individual

interposers 10 for use in the construction of packages 30 according to the present invention to save time and production costs. Actual dicing of the product 50 may occur at any stage of the processing of the interposer 10 such as, for example, after an interposer is populated with passive circuits and wired as described above, or following formation of the insulating layer 104 and prior to the formation of the passive circuits.

Once the package 30 has been fabricated it can be mounted on a larger circuit board and/or connected to other elements. The mounting of the package 30 may be accomplished by mechanical means well-known in the art, such as through the use of lead frames. Fig. 6 shows a lead frame 160 for carrying the completed package 30 having wire bonds or leads 162. The leads 162 of the lead frame 160 will connect to either the IC chips 20, 22 or the interposer 10 through wire bonds 138 or the chips and/or interposer can be, in part or in whole, directly bonded to the lead frame. In order to protect the interposer 10 and the IC chips 20, 22, the unit may be encapsulated by methods well-known in the art, such as through an epoxy encapsulation 164 or sealing in a container which is vacuum-sealed or filled with an inert gas.

Fig. 7 shows the implementation of the lead frame 160 containing the package 30 of the present invention within an integrated RF/digital communications system 40. Lead frame 160 is electrically connected to a circuit board 166 through leads 162. At least one lead 162 is connected through

conductor line 170 to an antenna 168 for receiving and sending RF signals which are processed by the package 30 contained within the lead frame 162.

With the present invention, the integration of RF analog circuit elements and digital circuit elements within a single circuit package which is compact and does not suffer from semiconductor substrate induced effect degradation is performed without the need to use mechanically weak constructs such as substrate air-bridges and without the need to use a non-semiconductor base for the implementation of passive circuit elements.

It should be readily understood that the invention is not limited to the specific embodiment described and illustrated above. Rather, the invention can be modified to incorporate any number of variations, alterations, substitutions or equivalent arrangements not heretofore described, which are commensurate with the spirit and scope of the invention. Accordingly, the invention is not limited by the foregoing description, but is only limited by the scope of the appended claims.

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A chip carrier comprising:

an interposer element comprising a semiconductor substrate layer and at least one insulating layer on a surface of said substrate layer, said insulating layer supporting at least one passive circuit element which is separated from said substrate layer by a portion of said insulating layer, said portion of said insulating layer having a thickness which is sufficient to electrically shield said at least one passive circuit element from said substrate layer.

2. The chip carrier of claim 1, further comprising at least one integrated circuit chip attached to said interposer element and electrically connected to said at least one passive circuit element.

3. The chip carrier of claim 2, wherein said semiconductor substrate layer comprises a silicon layer.

4. The chip carrier of claim 3, wherein said at least one insulating layer comprises an oxide layer.

5. The chip carrier of claim 4, wherein said oxide layer includes silicon dioxide ( $\text{SiO}_2$ ).

6. The chip carrier of claim 5, wherein said oxide layer has a thickness within a range of three to five microns.

7. The chip carrier of claim 3, wherein said at least one insulating layer comprises a polyamide layer.

8. The chip carrier of claim 3, wherein said at least one passive element is embedded within said at least one insulating layer.

9. The chip carrier of claim 3, wherein said at least one passive element is formed on said at least one insulating layer.

10. The chip carrier of claim 3, further comprising a metallization pattern on or within said insulating layer connected with said at least one passive circuit device.

11. The chip carrier of claim 3, wherein said at least one insulating layer includes a plurality of passive circuit elements, said plurality of passive circuit elements separated from said substrate layer by a portion of said at least one insulating layer, said portion of said at least one insulating layer having a thickness such that said plurality of passive circuit elements are electrically shielded from the conductance of said substrate layer.

12. The chip carrier of claim 11, wherein said plurality of passive circuit elements includes a resistor element.

13. The chip carrier of claim 12, wherein said resistor element is a thin film metal resistor.

14. The chip carrier of claim 13, wherein said plurality of passive circuit elements includes a capacitor element.

5 15. The chip carrier of claim 14, wherein said capacitor element is a thin film capacitor.

16. The chip carrier of claim 15, wherein said thin film capacitor includes a dielectric layer.

17. The chip carrier of claim 16, wherein said dielectric layer is an oxide  
10 composition.

18. The chip carrier of claim 16, wherein said dielectric layer is an oxide-nitride-oxide composition.

19. The chip carrier of claim 15, wherein said plurality of passive circuit elements includes an inductor element.

15 20. The chip carrier of claim 19, wherein said inductor element is a spiral inductor.



21. The chip carrier of claim 20, wherein said plurality of passive circuit elements form at least one passive circuit device, said passive circuit device having at least one of said plurality of passive circuit elements and electrically connected to said at least one integrated circuit chip.

5 22. The chip carrier of claim 21, wherein said plurality of passive circuit elements form at least one passive circuit device used in radio frequency (RF) communications systems.

23. The chip carrier of claim 22, wherein said interposer element and said at least one integrated circuit are arranged to form circuitry used in RF communications  
10 systems.

24. The chip carrier of claim 23, wherein said at least one passive circuit device comprises a load amplifier.

25. The chip carrier of claim 23, wherein said at least one passive circuit device comprises a broad band amplifier.

15 26. The chip carrier of claim 23, wherein said at least one passive circuit device comprises an oscillator.

27. The chip carrier of claim 26, wherein said oscillator is a voltage controlled oscillator.

28. The chip carrier of claim 23, wherein said at least one integrated circuit chip comprises a chip having at least one logic device electrically connected to said interposer element.

29. The chip carrier of claim 28, wherein said chip contains analog circuitry.

5 30. The chip carrier of claim 28, wherein said at least one logic device is a transistor.

31. The chip carrier of claim 30, wherein said chip contains digital circuitry.

32. The chip carrier of claim 31, wherein said chip is a microprocessor.

33. The chip carrier of claim 31, wherein said chip is a memory chip.

10 34. The chip carrier of claim 29, wherein said at least one integrated circuit chip is attached to said interposer element by solder joints.

35. The chip carrier of claim 34, wherein said at least one integrated circuit chip is attached to said interposer element through flip-chip bonding.

15 36. The chip carrier of claim 35, wherein said solder joints have varying compositions such that each of said solder joints has a selective melting temperature.

37. The chip carrier of claim 29, wherein said at least one integrated circuit chip is attached to said interposer element by a conductive adhesive substance.

38. The chip carrier of claim 29, wherein a bonding agent is located in the area between the said at least one integrated circuit chip and said insulating layer.

5 39. The chip carrier of claim 38, wherein said bonding agent is epoxy.

40. The chip carrier of claim 29, wherein said chip carrier is encapsulated to form a circuit package, said circuit package having conducting leads on an outer side of said package.

41. The chip carrier of claim 40, further comprising conductive leads  
10 connecting the chip carrier to said conductive package leads of said circuit package.

42. The chip carrier of claim 2, wherein said interposer element includes first and second insulating layers on opposing surfaces of said substrate.

43. The chip carrier of claim 42, wherein each of said first and second insulating layers has at least one passive circuit element separated from said substrate  
15 layer by a portion of said first and second insulating layers having a thickness such that each of said at least one passive circuit elements is electrically shielded from the conductance of said substrate layer.

44. The chip carrier of claim 43 wherein said first and second insulating layers include a plurality of passive circuit elements.

45. The chip carrier of claim 44, wherein at least one of said first and second insulating layers has at least one active circuit element.

46. The chip carrier of claim 1, wherein said substrate layer is comprised of gallium-arsenide.

47. The chip carrier of claim 46, wherein said insulating layer is comprised of gallium-arsenide-oxide.

48. A chip carrier comprising:

an interposer element comprising a semiconductor substrate layer and at least one insulating layer on a surface of said substrate layer, said insulating layer supporting at least one passive circuit element which is separated from said substrate layer by a portion of said insulating layer, said portion of said insulating layer having a thickness which is sufficient to electrically shield said at least one passive circuit element from said substrate layer;

at least one integrated circuit chip attached to said interposer element and electrically connected to said at least one passive circuit element; and

said interposer element and said at least one integrated circuit contain electrical elements which form circuitry for use in radio frequency (RF) communications systems.

49. The chip carrier of claim 48, wherein at least one of said plurality of  
5 insulating layers comprises an oxide layer.

50. The chip carrier of claim 49, wherein said oxide layer includes silicon dioxide ( $\text{SiO}_2$ ).

51. The chip carrier of claim 50, wherein said oxide layer has a thickness within a range of three to five microns.

52. The chip carrier of claim 48, wherein at least one of said plurality of  
10 insulating layers comprises a polyamide layer.

53. The chip carrier of claim 48, wherein at least one of said plurality of passive elements is embedded within said at least one insulating layer.

54. The chip carrier of claim 48, wherein at least one of said plurality of  
15 passive elements is formed on said at least one insulating layer.

55. The chip carrier of claim 48, further comprising a metallization pattern on or within said insulating layer connected with said at least one passive circuit device.

56. The chip carrier of claim 55, wherein said plurality of passive circuit elements includes a resistor element.

57. The chip carrier of claim 56, wherein said resistor element is a thin film metal resistor.

58. The chip carrier of claim 57, wherein said plurality of passive circuit elements includes a capacitor element.

59. The chip carrier of claim 58, wherein said capacitor element is a thin film capacitor.

60. The chip carrier of claim 59, wherein said thin film capacitor includes a dielectric layer.

61. The chip carrier of claim 60, wherein said dielectric layer is an oxide composition.

62. The chip carrier of claim 60, wherein said dielectric layer is an oxide-nitride-oxide composition.

63. The chip carrier of claim 60, wherein said plurality of passive circuit elements includes an inductor element.

64. The chip carrier of claim 63, wherein said inductor element is a spiral inductor.

65. The chip carrier of claim 64, wherein said plurality of passive circuit elements form at least one passive circuit device, said passive circuit device having at least one of said plurality of passive circuit elements and electrically connected to said at least one integrated circuit chip.

66. The chip carrier of claim 65, wherein said plurality of passive circuit elements form at least one passive circuit device used in radio frequency (RF) communications systems.

10 67. The chip carrier of claim 66, wherein said at least one passive circuit device comprises a load amplifier.

68. The chip carrier of claim 66, wherein said at least one passive circuit device comprises a broad band amplifier.

69. The chip carrier of claim 66, wherein said at least one passive circuit device comprises an oscillator.

70. The chip carrier of claim 69, wherein said oscillator is a voltage controlled oscillator.

71. The chip carrier of claim 66, wherein said at least one integrated circuit chip comprises a chip having at least one logic device electrically connected to said interposer element.

72. The chip carrier of claim 71, wherein said chip contains analog circuitry.

5 73. The chip carrier of claim 71, wherein said at least one logic device is a transistor.

74. The chip carrier of claim 73, wherein said chip contains digital circuitry.

75. The chip carrier of claim 74, wherein said chip is a microprocessor.

76. The chip carrier of claim 74, wherein said chip is a memory chip.

10 77. The chip carrier of claim 71, wherein said at least one integrated circuit chip is attached to said interposer element by solder joints.

78. The chip carrier of claim 77, wherein said at least one integrated circuit chip is attached to said interposer element through flip-chip bonding.

79. The chip carrier of claim 78, wherein said solder joints have varying  
15 compositions such that each of said solder joints has a selective melting temperature.



80. The chip carrier of claim 71, wherein said at least one integrated circuit chip is attached to said interposer element by a conductive adhesive substance.

81. The chip carrier of claim 71, wherein a bonding agent is located in the area between the said at least one integrated circuit chip and said insulating layer.

5 82. The chip carrier of claim 81, wherein said bonding agent is epoxy.

83. The chip carrier of claim 71, wherein said chip carrier is encapsulated to form a circuit package, said circuit package having conducting leads on an outer side of said package.

84. The chip carrier of claim 83, further comprising conductive leads  
10 connecting the chip carrier to said conductive package leads of said circuit package.

85. The chip carrier of claim 71, wherein said interposer element includes first and second insulating layers on opposing surfaces of said silicon substrate.

86. The chip carrier of claim 85, wherein each of said first and second insulating layers has a plurality of passive circuit elements separated from said silicon  
15 substrate layer by a portion of said first and second insulating layers having a thickness such that said plurality of passive circuit elements are electrically shielded from the conductance of said silicon substrate layer.

87. The chip carrier of claim 86, wherein at least one of said first and second insulating layers has at least one active circuit element.

88. A process for forming an interposer element for use as a chip carrier comprising the steps of:

5 providing an insulating layer on at least one surface of a silicon substrate;  
and

processing said insulating layer to produce at least one passive circuit  
element on or within said insulating layer, said at least one passive circuit element  
being separated from said silicon substrate by a portion of said insulating layer,  
10 said portion of said insulating layer having a thickness such that said at least one  
passive circuit element is electrically shielded from said silicon substrate.

89. The process according to claim 88, further comprising the step of  
bonding at least one integrated circuit chip to the interposer element such that said at  
least one integrated circuit chip is electrically connected to said at least one passive  
15 circuit element.

90. The process according to claim 89, wherein said step of bonding  
comprises solder bonding.

91. The process according to claim 90, wherein said step of bonding comprises flip-chip bonding.

92. The process according to claim 89, wherein said insulating layer is formed of an oxide.

5 93. The process according to claim 92, wherein said oxide is silicon dioxide ( $\text{SiO}_2$ ).

94. The process according to claim 93, wherein said insulating layer has a thickness within a range of three to five microns.

95. The process according to claim 89, wherein said insulating layer is formed  
10 of polyamide.

96. The process according to claim 89, further comprising the step of forming a metallization pattern on or within said insulating layer, said metallization pattern connected with said at least one passive circuit element.

97. The process according to claim 96, wherein said step of processing said  
15 insulating layer further comprises the step of producing a plurality of passive circuit elements on or within said insulating layer.

98. The process according to claim 97, wherein said plurality of passive circuit elements includes a resistor element.

99. The process according to claim 98, wherein said resistor element is a thin film metal resistor.

100. The process according to claim 97, wherein said plurality of passive circuit elements includes a capacitor element.

101. The process according to claim 100, wherein said capacitor element is a thin film capacitor.

102. The process according to claim 101, wherein said thin film capacitor includes a dielectric layer.

103. The process according to claim 102, wherein said dielectric layer is an oxide composition.

104. The process according to claim 102, wherein said dielectric layer is an oxide-nitride-oxide composition.

105. The process according to claim 97, wherein said plurality of passive circuit elements includes an inductor element.

106. The process according to claim 105, wherein said inductor element is a spiral inductor.

107. The process according to claim 97, further comprising the step of forming at least one passive circuit device for use in radio frequency (RF) communications systems, said passive circuit device having at least one of said plurality of passive circuit elements and electrically connected to said at least one integrated circuit chip.

108. The process according to claim 107, further comprising the step of arranging the interposer element and said at least one integrated circuit to form circuitry for use in RF communications systems.

109. The process according to claim 108, wherein said at least one passive circuit device is for use in a load amplifier.

110. The process according to claim 108, wherein said at least one passive circuit device is for use in a broad band amplifier.

111. The process according to claim 108, wherein said at least one passive circuit device is for use in an oscillator.

112. The process according to claim 111, wherein said oscillator is a voltage controlled oscillator.

113. The process according to claim 108, wherein said at least one integrated circuit chip contains analog circuitry.

114. The process according to claim 108, wherein said at least one integrated circuit chip contains digital circuitry.

115. The process according to claim 114, wherein said integrated circuit chip is a microprocessor.

116. The process according to claim 114, wherein said integrated circuit chip is a memory chip.

117. The process according to claim 108, further comprising the step of forming a bonding layer, said bonding layer located in the area between said at least one integrated circuit chip and said insulating layer.

118. The process according to claim 117, wherein said bonding agent is epoxy.

119. The process according to claim 118, further comprising the step of encapsulating the interposer element and said at least one integrated circuit to form a circuit package, said circuit package having conducting leads on an outer side of said package.

120. The process according to claim 119, further comprising the step of providing conductive leads connecting the interposer element and said at least one integrated circuit to said conductive package leads of said circuit package.

121. The process according to claim 120, further comprising the step of  
5 providing an insulating layer to both surfaces of said silicon substrate.

122. The process according to claim 121, further comprising the step of processing said insulating layer to produce at least one active circuit element.

123. The process according to claim 88, said step of processing said insulating layer further comprising the step of providing at least one passive circuit element in each  
10 of a plurality of areas of said insulating layer, dividing said silicon substrate into said areas, and bonding at least one integrated circuit chip to each of said areas of said insulating layer to form respective chip carriers.

**ABSTRACT**

An apparatus is provided for the supply of passive electronic components to a chip containing circuitry capable of operating in a communications system. The invention provides a silicon interposer element chip package which includes a silicon substrate and which is capable of carrying one or more IC chips and which does not suffer semiconductor leeching problems. A silicon substrate is formed from a silicon layer and an insulating layer, preferably an oxide. The invention also provides passive circuits within the interposer element oxide layer. The interposer element is then bonded to an integrated circuit chip using flip-chip processing.



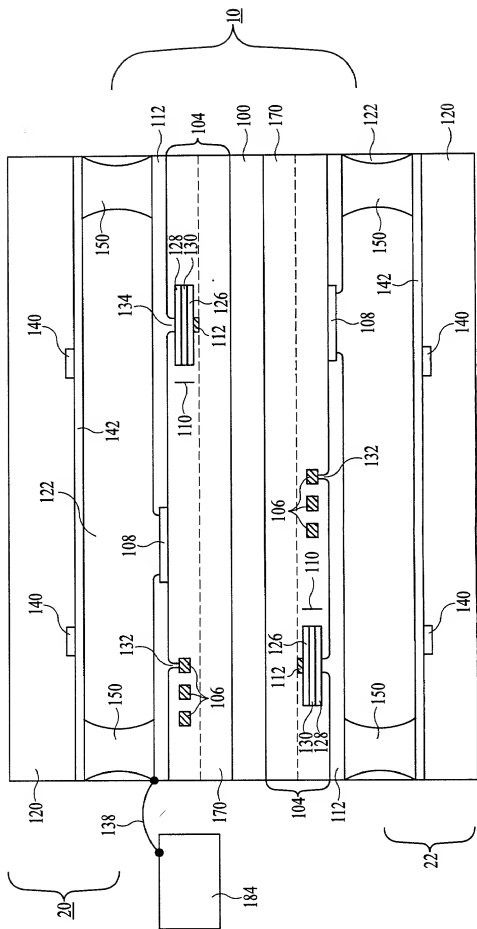


FIG. 1

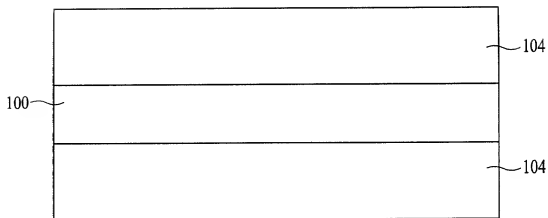


FIG. 2a

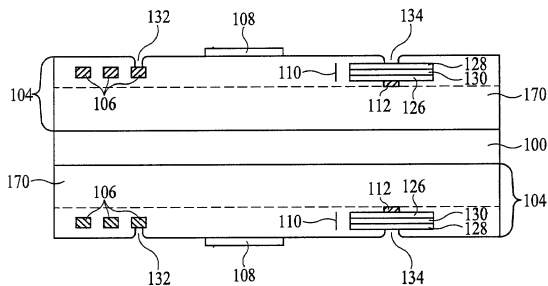


FIG. 2b

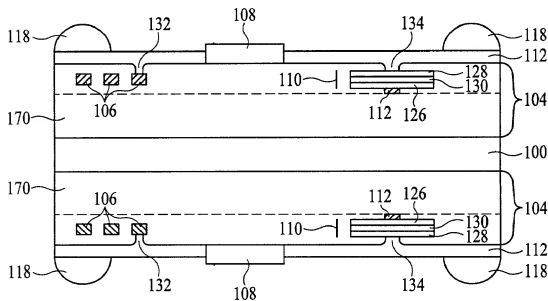


FIG. 2c

20

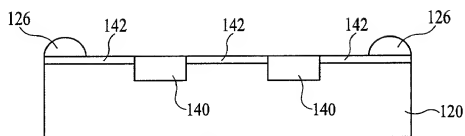


FIG. 3

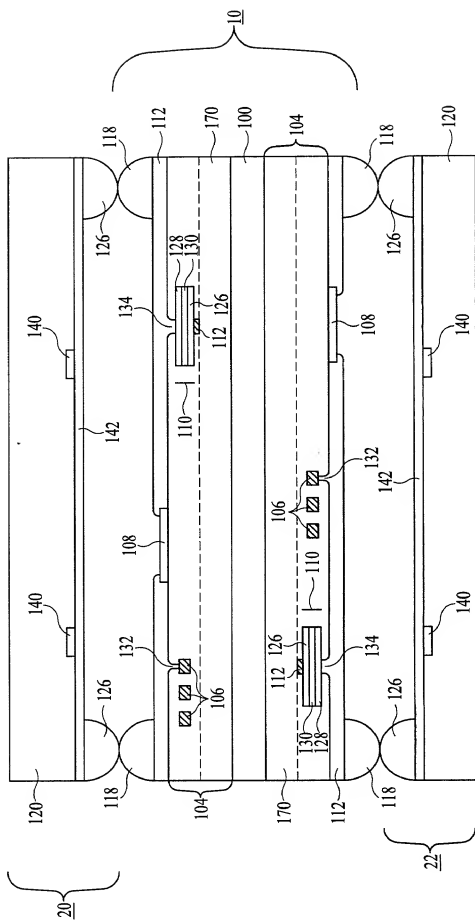


FIG. 4



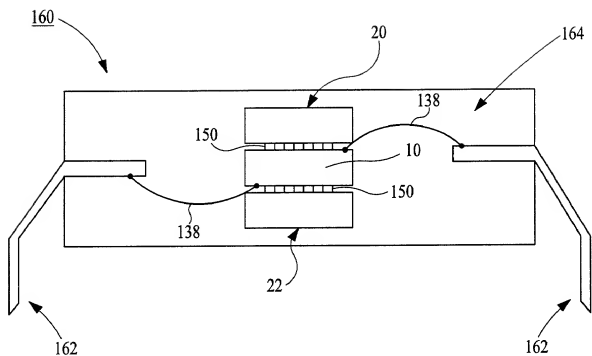


FIG. 6

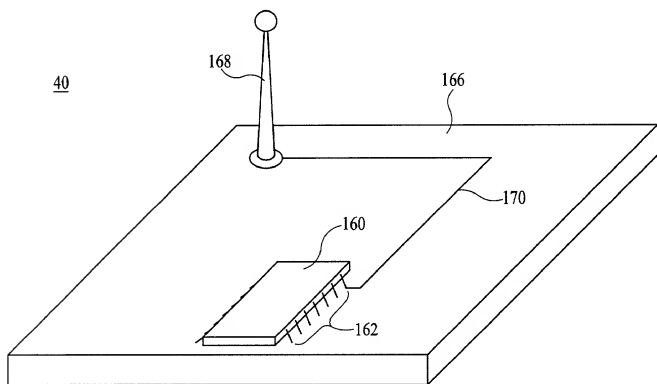
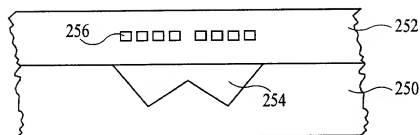
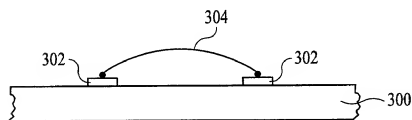


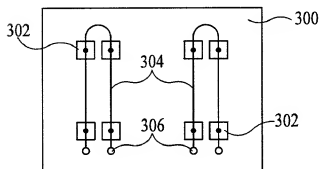
FIG. 7



**FIG. 8**  
**PRIOR ART**



**FIG. 9a**  
**PRIOR ART**



**FIG. 9b**  
**PRIOR ART**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**DECLARATION FOR PATENT APPLICATION**

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

**SILICON MULTI-CHIP MODULE PACKAGING WITH INTEGRATED  
PASSIVE COMPONENTS AND METHOD OF MAKING**

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/356 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

None

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

None



I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Please address all correspondence to Thomas J. D'Amico of Dickstein Shapiro Morin & Oshinsky LLP located at 2101 L Street NW, Washington, DC 20037-1526. Telephone calls should be made to Thomas D'Amico by dialing (202) 828-2232.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**DECLARATION FOR PATENT APPLICATION**

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

**SILICON MULTI-CHIP MODULE PACKAGING WITH INTEGRATED  
PASSIVE COMPONENTS AND METHOD OF MAKING**

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/356 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

None

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

None

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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PATENT

Docket No.: M4065.127/P127

Micron No.: 98-0747

**IN THE UNITED STATES  
PATENT AND TRADEMARK OFFICE**

Patent Application

Inventors: Kie Y. Ahn et al.

Serial No.: Not Yet Assigned

Group Art Unit: Not Yet  
Assigned

Filed: Concurrently Herewith

Examiner: Not Yet Assigned

For: SILICON MULTI-CHIP  
MODULE PACKAGING WITH  
INTEGRATED PASSIVE  
COMPONENTS AND METHOD  
OF MAKING

**POWER OF ATTORNEY BY ASSIGNEE AND  
CERTIFICATE BY ASSIGNEE UNDER 37 CFR § 3.73(b)**

Micron Technology, Inc., assignee of the entire right, title and interest in the above-identified application by virtue of the assignment attached hereto (which is also being submitted concurrently for recordation), hereby appoints the attorneys and agents of the firm of Dickstein Shapiro Morin & Oshinsky LLP located at 2101 L Street, NW, Washington, DC 20037-1526, listed as follows: Gary M. Hoffman, 26,411; Thomas J. D'Amico, 28,371; Donald A. Gregory, 28,954; James W. Brady, Jr., 32,115; Jon D. Grossman, 32,699; Mark J. Thronson, 33,082; Laurence D. Fisher, 37,131; John R. Fuisz, 37,327; James M. Heintz, P41,828; June Cohan Lazar, P43,741; Brian Lemm, P43,748; Gianni Minutoli, 41,198; Eric Oliver, 35,307; William E. Powell, III, 39,803; James M.

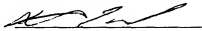
Silbermann, 40,413; Richard Veltman, 36,957; and also attorneys Michael L. Lynch, 30,871; Lia M. Pappas, 34,095; W. Eric Webostad, 35,406; and Charles B. Brantley, II, 38,086 of Micron Technology, Inc. as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

The assignee certifies that the above-identified assignment has been reviewed and to the best of the assignee's knowledge and belief, title is in the assignee.

Please direct all correspondence regarding this application to the following:

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